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Single-chip Massively Parallel Analog-to-Digital Conversion

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ABSTRACT OF THE DISCLOSURE

A circuit includes an input terminal coupled to receive an analog input signal, a multiple number of sample-and-hold circuits and a multiple number of analog-to-digital (A/D) converters. The input terminal of each of the sample-and-hold circuits is coupled to receive the analog input signal. Each of the A/D converters has an input terminal and an output terminal, where the input terminal is coupled to an output terminal of a corresponding one of the sample-and-hold circuits. In operation, the sample-and-hold circuits sample the analog input signal sequentially and store a multiple number of analog samples at each of the sample-and-hold circuits. The A/D converters convert the analog samples in parallel to generate digital values at the output terminals of each of the A/D converters representative of each of the analog samples. In one embodiment, the A/D converters are implemented based on a multi-channel bit-serial (MCBS) analog-to-digital conversion scheme.